ABSTRACT

An apparatus and method for verifying a logic function of a semiconductor chip in a logic chip emulation environment where a processing engine and a target interface engine interact with each other. The apparatus in accordance with the present invention generally includes a processing engine for executing a software algorithm corresponding to the logic design of the target chip, and a target interface engine interfacing with the target system for transmitting/receiving pin signals to/from the target system. The software algorithm has one or more software variables, and the transmission/reception of the pin signals by the target interface engine occurs with the execution of the software algorithm by the processing engine. The software variable and the pin signals are time-variant with the execution of the algorithm. The processing engine comprises means for finding correspondence between the software variables and the pin signals at a predetermined time, so that the values of the software variables and the values of the hardware pin signals corresponding in time thereto can be monitored in synchronization with each other.